

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

Applicant(s): T. Sekiguchi, et al.

Filed: March 29, 2004

For: METHOD OF MANUFACTURING SEMICONDUCTOR  
INTEGRATED CIRCUIT DEVICES HAVING A MEMORY  
DEVICE WITH REDUCED BIT LINE STRAY CAPACITY AND  
SUCH SEMICONDUCTOR INTEGRATED CIRCUIT DEVICES

**CLAIM FOR PRIORITY**

Mail Stop Patent Application  
Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

March 29, 2004

Sir:

Pursuant to the provisions of 35 USC § 119 and 37 CFR § 1.55, Applicants  
hereby claim the right of priority based on Japanese Patent Application  
No. 8-135534, filed in Japan on May 29, 1996.

A certified copy of the above-identified Japanese Patent Application was  
submitted on May 23, 1997, in prior Application No. 08/862,320, filed  
May 23, 1997.

Respectfully submitted,

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